UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/441,038	04/06/2012	Rolf Weis	1012-0388 / 2011P51343US	8402

57579 7590 12/12/2016

MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

EXAMINER
BRASFIELD, QUINTON A

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
12/12/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

official@mbhiplaw.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte ROLF WEIS and
ANDREAS SPITZER

Appeal 2015-004593
Application 13/441,038[1]
Technology Center 2800

Before ADRIENE LEPIANE HANLON, CATHERINE Q. TIMM, and JAMES C. HOUSEL, *Administrative Patent Judges*.

PER CURIAM.

DECISION ON APPEAL

A. STATEMENT OF THE CASE

Appellants filed an appeal under 35 U.S.C. § 134(a) from the Examiner's decision finally rejecting claims 1–25. We have jurisdiction under 35 U.S.C. § 6(b).[2]

---

[1] According to Appellants, the real party in interest is Infineon Technologies AG. App. Br. 2.

[2] Our decision refers to the Specification filed Dec. 20, 2012 (Spec.), the Final Office Action (Final Act.) mailed April 29, 2014, the Advisory Action mailed July 24, 2014 (Adv. Act), Appellants' Appeal Brief (Appeal Br.) filed Sept. 26, 2014, the Examiner's Answer (Ans.) mailed Jan. 16, 2015, and Appellants' Reply Brief (Reply Br.) filed Mar. 13, 2015.

We REVERSE.

The claims on appeal are directed to integrated circuits (*see, e.g.*, claims 1, 24, and 25). Appellants disclose that integrated switching devices, such as power transistors, are widely used in industrial, automotive, or consumer applications for various types of loads. Spec. ¶ 2. It is desirable in some applications to limit the voltage across a load path of a transistor to a voltage below the voltage blocking capability of the transistor so the transistor is not operated in a breakdown mode. Spec. ¶ 4. Although transistors functioning as a switching device typically possess an intrinsic body diode, it is undesirable to use the intrinsic body diode as a freewheeling diode because the electrical properties of the intrinsic body diode are not independent from the electrical properties of the transistor as a switching device. App. Br. 5; Spec. ¶ 32. To address this, Appellants disclose connecting a rectifier in parallel with at least one section of a load path of a switching device. Appellants' Figure 2 is reproduced below.

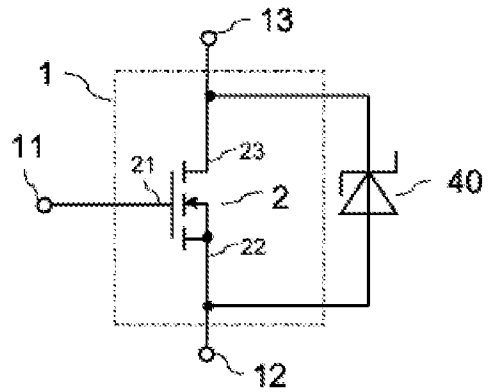

FIG 2

Figure 2 depicts an integrated circuit including a switching device

A switching device 1 includes a first switching element 2, a control terminal 11, a first load terminal 12, and a second load terminal 13. Spec. ¶ 33. The first

switching element 2 can be a transistor having a control terminal 21, a first load terminal 22, and a second load terminal 23. *Id.* A rectifier element 40 is connected in parallel with the switching element 2. *Id.* at ¶ 34. Although the switching element 2 has a voltage blocking capability, the rectifier element 40 may have a breakdown voltage lower than the switching element 2 so the rectifier element 40 prevents a voltage between load terminals 12 and 13 from attaining the breakdown voltage of the switching element 2, thus protecting the switching element 2. *Id.* at ¶¶ 31, 34.

Appellants disclose an embodiment of a semiconductor body in which a switching device and a rectifier element are integrated. Appellants' Figure 5 is reproduced below.

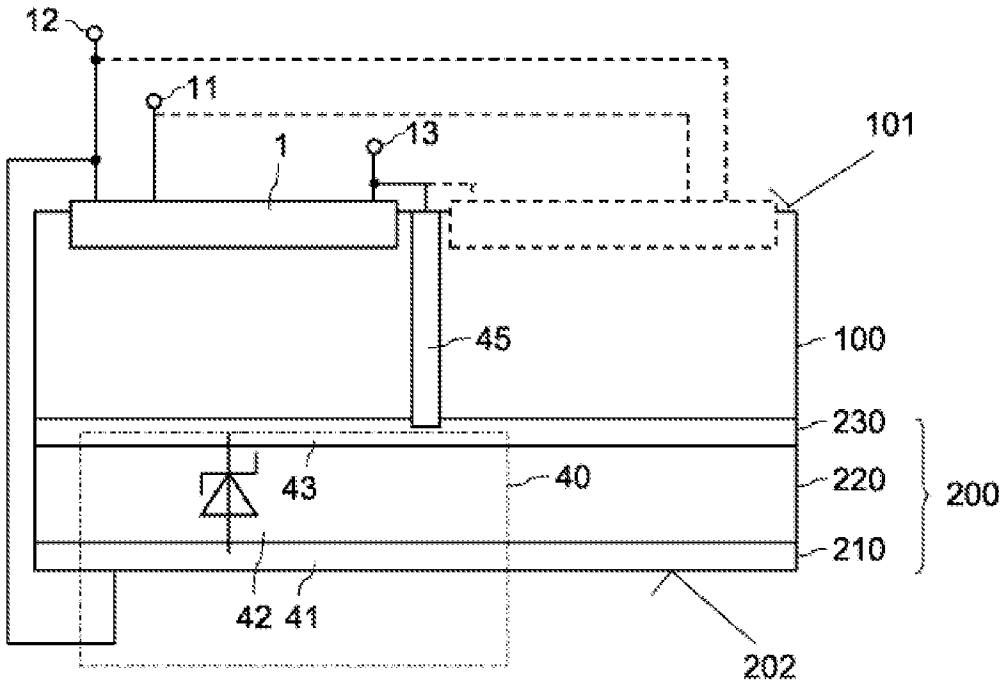

FIG 5

Figure 5 is a vertical cross sectional view of a semiconductor body

The semiconductor body includes a first semiconductor layer 100 in which a switching device 1 is integrated and a second semiconductor layer 200 in which a rectifier element 40 is integrated. Spec. ¶ 58. The second semiconductor layer 200 is adjacent the first semiconductor layer 100 in a vertical direction of the semiconductor body, which is a direction perpendicular to a first surface 101 of the first semiconductor layer 100. *Id.* Appellants disclose that a switching element (e.g., switching element 2 of switching device 1 of Figure 2 above) is a lateral device having a load path extending in a lateral direction (i.e., along a direction parallel to first surface 101 of the first semiconductor layer 100. Spec. ¶ 59.

Independent claim 1 is illustrative and is reproduced below from the Claims Appendix of the Appeal Brief. The limitations at issue are italicized.

> 1. An integrated circuit comprising:
> a semiconductor body with a first semiconductor layer and a second semiconductor layer arranged adjacent the first semiconductor layer in a vertical direction of the semiconductor body;
> a switching device with a control terminal and a load path between a first load terminal and a second load terminal;
> a rectifier element connected in parallel with at least one section of the load path;
> *wherein the switching device is integrated in the first semiconductor layer* and the rectifier element is integrated in the second semiconductor layer; and
> *wherein the load path of the switching device extends in a lateral direction of the first semiconductor layer.*

App. Br. 27.

The claims on appeal stand rejected as follows:

(1) claims 1 and 16 under 35 U.S.C. § 102(b) as being anticipated by

Otremba;[3]

(2) claims 2–15 under 35 U.S.C. § 103(a) as unpatentable over the combination of Otremba in view of Fallica;[4]

(3) claim 17 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Otremba in view of Shinoda;[5]

(4) claim 18 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Otremba in view of Brubaker;[6]

(5) claims 19 and 21 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Otremba and Shinoda and further in view of Brubaker;

(6) claim 20 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Otremba and Shinoda and further in view of Brubaker and Hu;[7]

(7) claims 22 and 23 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Otremba and Shinoda and further in view of Brubaker and Adan;[8]

(8) claim 24 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Schulze[9] in view of Otremba and Fallica; and

(9) claim 25 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Otremba in view of Eckardt[10] and Haerle.[11]

---

[3] Otremba, US 2009/0273913 A1, published Nov. 5, 2009 ("Otremba").
[4] Fallica, US 6,559,505 B1, issued May 6, 2003 ("Fallica").
[5] Shinoda et al., US 2011/0227630 A1, published Sept. 22, 2011 ("Shinoda").
[6] Brubaker et al., US 2012/0274496 A1, published Nov. 1, 2012 ("Brubaker").
[7] Hu, US 2006/0052947 A1, published Mar. 9, 2006 ("Hu").
[8] Adan, US 2005/0282342 A1, published Dec. 22, 2005 ("Adan").
[9] Schulze et al., US 2011/0024791 A1, published Feb. 3, 2011 ("Schulze").
[10] Eckardt et al., US 7,466,020 B2, issued Dec. 16, 2008 ("Eckardt").
[11] Haerle et al., US 2006/0192599 A1, published Aug. 31, 2006 ("Haerle").

B. DISCUSSION

1. Rejection of claims 1 and 16 over Otremba

Claims 1 and 16 are rejected under 35 U.S.C. § 102(b) as being anticipated by Otremba. We select claim 1 as representative for discussing the issues on appeal.

The Examiner finds Otremba discloses a semiconductor body including a first semiconductor layer and a second semiconductor layer, citing Figure 1 and the first semiconductor body 120 and second semiconductor body 140 shown in Figure 3A of Otremba. Final Act. 2. Citing the first semiconductor switching element 20 and freewheeling element 40 disclosed by Otremba, the Examiner finds Otremba respectively discloses a switching device and a rectifier element in parallel with at least one section of the switching device's load path. *Id.* at 3. Citing the first load path connections 21, 31 shown in Figure 1 and citing paragraph 40 of Otremba, the Examiner finds a load path of a switching device extends in a lateral direction of the first semiconductor layer. *Id.* Thus, the Examiner appears to rely on paragraph 40 and Figures 1 and 3A of Otremba for an express disclosure of a switching device having a load path extending in a lateral direction of a first semiconductor layer, as recited in claim 1.

Appellants contend Otremba does not disclose a switching device having a load path extending in a lateral direction of a first semiconductor layer, as recited in claim 1. Appeal Br. 13. Specifically, Appellants argue Otremba discloses a vertical device because paragraph 40 of Otremba describes a first load path connection on a first surface 121 of the semiconductor body 120 and a second load path connection on a second surface 122 of the semiconductor body 120. *Id.* at 14. Thus, the load path of the switching element 20 extends in a vertical direction between surfaces 121, 122. *Id.* at 14–15.

Appellants' arguments are persuasive of reversible error. Appellants have explained that paragraph 40 of Otremba does not support the Examiner's finding that Otremba expressly discloses a switching device having a load path extending in a lateral direction of a first semiconductor layer, as recited in claim 1, because paragraph 40 describes a vertical device having load path connections arranged along a vertical direction. In response to Appellants' arguments regarding paragraph 40 of Otremba, the Examiner only reiterates the finding that paragraph 40 discloses a load path extending in a lateral direction of a first semiconductor layer. Ans. 4. This is insufficient to refute Appellants' arguments and explanation.

With regard to a position taken by the Examiner in the Advisory Action that Figures 1 and 3A of Otremba depict top views of a semiconductor device so the load path of switching devices 20, 30 extend in a lateral direction between terminals 11, 12, Appellants contend this load path includes two switching devices 20, 30 integrated in different semiconductor bodies, which cannot disclose a switching device integrated in a first semiconductor layer and having the load path of claim 1. Appeal Br. 17–18.

This argument is also persuasive of reversible error. Figure 1 of Otremba is reproduced below.

FIG 1

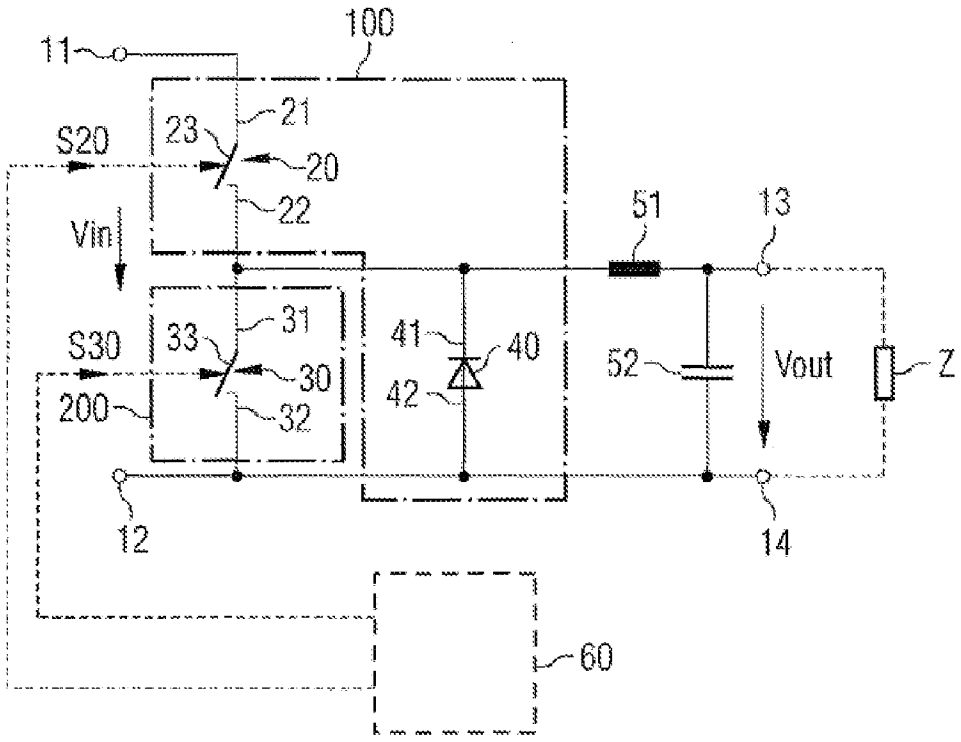

Figure 1 depicts a circuit diagram for a switching converter

As indicated in Figure 1, a first semiconductor switching element 20 and a rectifier element 40 are arranged in a first chip housing 100. Otremba ¶ 38. A second semiconductor switching element 30 is arranged in a second chip housing 200. *Id.* As shown in Figure 1, a load path across input terminals 11 and 12 would include the first semiconductor switching element 20 and the second semiconductor switching element 30. However, as argued by Appellants, this load path includes two semiconductor switching elements 20, 30 integrated in different switching devices. Figure 3A of Otremba is reproduced below.

FIG 3A

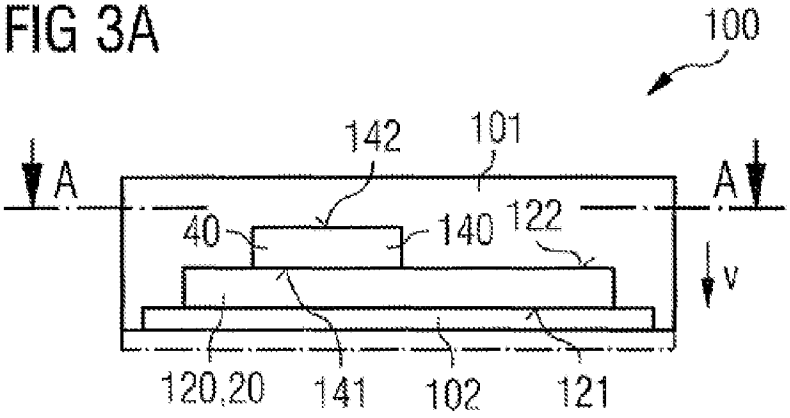

Figure 3A depicts a cross section of a first chip housing

Figure 3A depicts a cross-section of the first chip housing 100. Otremba ¶ 39. The first semiconductor switching element 20 is integrated in a first semiconductor body 120 and the rectifier element 40 is integrated in a second semiconductor body 140. *Id.* As indicated by Appellants,[12] the first semiconductor body 120 may correspond to the first semiconductor layer of claim 1, which includes a switching device (i.e., first semiconductor switching element 20) and is adjacent to a second semiconductor layer (i.e., second semiconductor body 140) in a vertical direction, wherein a rectifier element (i.e., rectifier element 40) is integrated in the second semiconductor layer. However, the load path identified by the Examiner[13] extends between input terminals 11, 12, or at least between first load path connections 21, 31,[14] which extend through first semiconductor switching element 20 and second semiconductor switching element 30. As indicated in Figure 1, the second semiconductor switching element 30 is arranged in a second chip housing 200. Otremba ¶ 38. Therefore, the second

[12] Appeal Br. 18.
[13] Ans. 3.
[14] Final Act. 3; Ans. 4.

semiconductor switching element 30 is not a switching device integrated in a first semiconductor layer (i.e., first semiconductor body 120 of the first chip housing 100) adjacent a second semiconductor layer (i.e., second semiconductor body 140), in which a rectifier element is integrated, and having a load path extending in a lateral direction of the first semiconductor layer (i.e., first semiconductor body 120), as recited in claim 1.

To the extent the Examiner finds the first semiconductor switching element 20 is the switching element of claim 1 and provides a portion of the load path between terminals 11 and 12, the first semiconductor switching element 20 does not provide the lateral load path of claim 1. As explained by Appellants,[15] paragraph 40 of Otremba describes a vertical device having a first load path connection at a first surface 121 of the semiconductor body 120 and a second load path connection at a second surface 122 of the semiconductor body 120. These load path connections at surfaces 121, 122 are arranged along a vertical direction, as shown in Figure 3A.

Moreover, the record does not support the Examiner's finding that Figures 1 and 3A provide top views of a semiconductor device. Ans. 4. Figure 1 depicts a circuit diagram for a switching converter[16] and does not explain whether the view is from the top or the side. Therefore, Figure 1 of Otremba does not indicate whether a load path of a switching device extends in a lateral direction of a first semiconductor layer. Otremba discloses Figure 3A is a cross-sectional view of a first chip housing 100 with a vertical direction indicated by letter "v." *Id.* at ¶ 43. As shown above, the arrow for v in Figure 3A extends along the plane of the page, not in and out of the page, as for a top view. Therefore, Figure 3A is a side cross-

[15] Appeal Br. 14–16.
[16] Otremba ¶ 20.

sectional view indicating first semiconductor body 120 and second semiconductor body 140 arranged along a vertical direction v.

At page 4 of the Answer, the Examiner finds "current not only travels in a lateral diredtion, [sic] but also the current travels in both devices in a vertical direction since the device is three-dimensional." Appellants respond by contending current is a flow of electrical carriers between regions of potential difference. Reply Br. 3. The regions of potential difference in the first switching device 20 of Otremba are at load connection pads 123, 124, which are spaced apart along a vertical direction. *Id.* In other words, the disclosure of Otremba does not support the Examiner's finding.

Appellants' arguments are persuasive of reversible error. "To anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or inherently." *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Robertson,* 169 F.3d 743, 745 (Fed. Cir. 1999) (citations and internal quotation marks omitted). Here, the Examiner relies upon the possibility or probability of current flowing along a lateral flow path. To rely upon a theory of inherency, there must be "a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (BPAI 1990). The Examiner has not provided any basis in the disclosure of Otremba or any technical reasoning to support a finding of a lateral flow path for the first semiconductor switching element 20. As explained by Appellants, the disclosure of Otremba describes a vertical load path

between the first and second load path connections for the first semiconductor switching element 20.

For the reasons discussed above, the rejection of claims 1 and 16 over Otremba is not sustained.

2. Rejections of claims 2–15 and 17–23 under 35 U.S.C. § 103

The § 103 rejections of claims 2–15 and 17–23 include Fallica, Shinoda, Brubaker, Hu, and Adan as additional references but include the same deficiencies as the § 102 rejection of claim 1 over Otremba. Although the § 103 rejections for claims 2–15 and 17–23 rely on additional prior art references, the Examiner does not rely on these added references to remedy the deficiencies in the § 102 rejection over Otremba. Therefore, we do not sustain the § 103 rejections of claims 2–15 and 17–23.

3. Rejection of claim 24 under 35 U.S.C. § 103

Independent claim 24 recites an integrated circuit comprising, among other things, a semiconductor body with a first semiconductor layer and a second semiconductor layer adjoining the first semiconductor layer such that a pn junction is formed between the first and second semiconductor layers, a switching device, and a rectifier element, "wherein the switching device is integrated in the first semiconductor layer and the rectifier element is integrated in the second semiconductor layer."

Claim 24 is rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Schulze in view of Otremba and Fallica. The Examiner finds Schulze discloses an integrated circuit comprising a semiconductor body having a first semiconductor layer and a second semiconductor layer adjoining the first

semiconductor layer in a vertical direction and forming a pn junction with the first semiconductor layer. Final Act. 12. The Examiner finds a rectifier element is integrated in the second semiconductor layer but Schulze does not disclose, among other things, a switching device integrated in the first semiconductor layer. *Id.*

Citing Figures 1 and 3A, the Examiner finds Otremba discloses an integrated circuit including a semiconductor body having first and second semiconductor layers, a switching device integrated in the first semiconductor layer, and a rectifier element integrated in the second semiconductor layer. *Id.* at 13. The Examiner concludes it would have been obvious to modify the device of Schulze to integrate a switching device in the first semiconductor layer. *Id.* at 13–14 (citing Otremba ¶¶ 37, 38).

Appellants assert Otremba does not provide a disclosure to motivate one of ordinary skill in the art to integrate a switching device into a semiconductor layer of Schulze. Appeal Br. 20. Appellants argue:

> In the Otremba reference, two discrete semiconductor **chips** are used in a vertical arrangement, with one chip being a switching device and another chip being a rectifier element. See, e.g., Otremba Fig. 3A; paragraph [0039] ("the semiconductor body 120 of the switching element and the semiconductor body 140 of the rectifier element are arranged one above another using chip-on-chip technology").

Id. 19–20.

Appellants argue that "Otremba's discrete semiconductor chips 20, 40 are not interchangeable with Schulze's semiconductor regions 1 and 2" wherein Otremba's chips 20, 40 "include electrically conductive pads at the top and bottom surfaces." *Id.* 20. Thus, according to Appellants:

> Otremba does not provide a useful teaching that would motivate or allow a person having ordinary skill to **integrate** a switching device into Schulze's semiconductor region 2. Although a person of ordinary skill might glean from Otremba that another **chip** could be stacked on

> top or below Schulze's device to form a vertical arrangement of a switching device and rectifier element, this does not produce the claimed structure [which recites that first and second semiconductor layers are arranged adjacent to one another].

Id.

In response, the Examiner finds Otremba's discrete semiconductor chips 20, 40 are interchangeable with Schulze's semiconductor regions 1, 2, because Otremba's chips 20, 40 and Schulze's regions 1, 2 are both "semiconductor layers." Ans. 5. However, merely characterizing Otremba's chips and Schulze's regions as "semiconductor layers" does not address the structural differences between Otremba's chips and Schulze's regions. *Compare* Otremba Fig. 3A (depicting discrete chips 20, 40) *with* Schulze Fig. 1 (depicting semiconductor device 100 comprising epitaxial layer or layers 40 accommodating p-type first semiconductor region 1 and n-type second semiconductor region 2); *see also* Schulze ¶ 32.

Based on the record before us, the Examiner's finding that Otremba's semiconductor chips 20, 40 and Schulze's regions 1, 2 are interchangeable is not supported by a preponderance of the evidence, and Appellants' arguments are persuasive of reversible error. The Examiner does not rely upon the disclosure Fallica to remedy this deficiency.[17] Therefore, we do not sustain the Examiner's rejection of claim 24 under 35 U.S.C. § 103(a).

[17] The Examiner relies upon Fallica for a disclosure of a first connector that is internal to a semiconductor body and between a rectifier element and a switching device. Final Act. 14–15.

4. Rejection of claim 25 under 35 U.S.C. § 103

Claim 25 recites an integrated circuit comprising, among other things, a semiconductor body including "a first semiconductor layer and a second semiconductor layer arranged adjacent the first semiconductor layer in a vertical direction of the semiconductor body," a switching device, and a rectifier element connected in parallel with at least one section of a load path of the switching device, "wherein the switching device is integrated in the first semiconductor layer and the rectifier element is integrated in the second semiconductor layer."

Claim 25 is rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Otremba in view of Eckardt and Haerle.[18] The Examiner finds Otremba discloses a semiconductor body including a first semiconductor layer and a second semiconductor layer arranged adjacent to the first semiconductor in a vertical direction of the semiconductor body. Adv. Act. 3. The Examiner further finds Otremba discloses a rectifier element connected in parallel with at least one section of a load path of a switching device, citing rectifier element 40 and the first load path connection 31 for the second semiconductor switching element 30 of Otremba. *Id.*

Appellants contend that although the second semiconductor switching element 30 is connected in parallel with the rectifier element 40, the second semiconductor switching element 30 is provided in a separate chip housing 200 from the chip housing 100 which includes the first semiconductor switching

[18] The Final Office Action rejects claim 25 under 35 U.S.C. § 103(a) over the combination of Otremba and Haerle. Final Act. 15–16. However, claim 25 is listed as rejected under 35 U.S.C. § 103(a) over the combination of Otremba, Eckardt, and Haerle in the Advisory Action. Adv. Act. 3. Appellants recognize that the Examiner relies upon Eckardt. App. Br. 23. Thus, our review is of the rejection over the combination of Otremba, Eckardt, and Haerle.

element 20 and the rectifier element 40. Appeal Br. 24. Therefore, the second semiconductor switching element 30 cannot be a switching device integrated in a first semiconductor layer arranged adjacent to a second semiconductor layer in which a rectifier element is integrated, as recited in claim 25. In addition, although the first semiconductor switching element 20 is arranged in a first semiconductor layer (i.e., first semiconductor body 120) adjacent, along a vertical direction, to a second semiconductor layer (i.e., second semiconductor body 140) in which the rectifier element 40 is arranged, the first semiconductor switching element 20 is arranged in series with the rectifier element 40. *Id.* at 24–25. Therefore, Otremba does not disclose a switching device integrated in a first semiconductor layer arranged adjacent, along a vertical direction, to a second semiconductor layer in which a rectifier element is integrated, wherein the rectifier element is connected in parallel with at least one section of a load path of the switching element, as recited in claim 25. *Id.* at 25.

Appellants' arguments are persuasive. In the Answer, the Examiner merely reiterates the findings in the Advisory Action, including the finding that the rectifier element 40 of Otremba is connected in parallel with at least one section of a load path, citing the first load path connection 31 for switching element 30. Ans. 7–8. The Examiner also finds Eckardt discloses a first semiconductor layer containing a switching device stacked vertically with a second semiconductor layer containing a rectifier element. *Id.* at 8. However, the Examiner does not find that Eckardt's rectifier element is connected in parallel with at least one section of a load path of the switching element, as recited in claim 25. Adv. Act. 3. Therefore, the Examiner does not rely on Eckardt to remedy the deficiencies of Otremba. The Examiner also does not rely on Haerle to remedy the deficiencies of Otremba. *Id.* (finding that Haerle discloses a switching device having a control terminal, a first

load terminal, and a second load terminal all accessible at first surface of a first semiconductor layer).

For the reasons set forth above, the § 103 rejection of claim 25 is not sustained.

C. DECISION

The decision of the Examiner is reversed.

REVERSED